ANDIJAN STATE PEDAGOGICAL INSTITUTE

Lecture materials · 2026–2027 academic year

SUBJECT

Information Systems and Digital Technologies

Lecture 3 · Understanding Computer Technology

Part 1 of 2 · 2 hours

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LECTURE 03 · 2 HOURS · PART 1/2

2

CHAPTER TWO

Fundamentals of Computers

Computer Organisation and Architecture

Inside the processor · how it talks to memory and devices · what an instruction really is

- The CPU and its units
- Memory & registers
- Machine cycle & buses
- CISC and RISC

WARM-UP

Your computer just worked out 2 + 2. How many separate steps did that take?

Write down a number before we start. By the end of this lesson you will be able to name every step.

1

Where was the instruction kept before it ran?

2

Which part of the CPU actually did the addition?

3

Where did the answer 4 go afterwards?

LEARNING OBJECTIVES

By the end of this lesson you will be able to…

1. Distinguish computer architecture from computer organisation, and give an example of each.
2. Name the units inside the CPU and the memory subsystems it uses, and state what each one does.
3. List the six CPU registers and say what each one holds.
4. Sequence the four phases of the machine cycle and the steps of a memory read and a memory write.
5. Explain how the processor communicates with memory and with I/O devices through the interface unit.

01

Architecture, Organisation and the CPU

Two related ideas · the block diagram · the CPU cycle · the three units inside the processor

- Architecture vs organisation
- Block diagram
- The CPU cycle
- AU · LU · CU

Two different but related ideas

WHAT IT IS

Computer architecture

The definition of the basic attributes of hardware components and their interconnections, in order to achieve specified goals in functions and performance.

- It defines the logical structure of a computer system
- Attributes include the instruction set, data representation and I/O mechanisms

HOW IT IS BUILT

Computer organisation

The design and physical arrangement of the various hardware units so that they work in tandem, in an orderly manner, to achieve the goals specified in the architecture.

- For one architecture there can be many different models
- Each model is a different organisation, depending on cost, physical size and technology used

The short version: architecture is the plan, organisation is the build. The architecture says what the machine must be able to do; the organisation decides how the hardware is arranged to do it.

CHECK FOR UNDERSTANDING

Sort it · architecture or organisation?

Which of the two ideas does each statement belong to?

1

“The processor must support this instruction set.”

Statement 1

2

“Use a cheaper chip and a smaller board in the budget model.”

Statement 2

3

“It defines the logical structure of the computer system.”

Statement 3

4

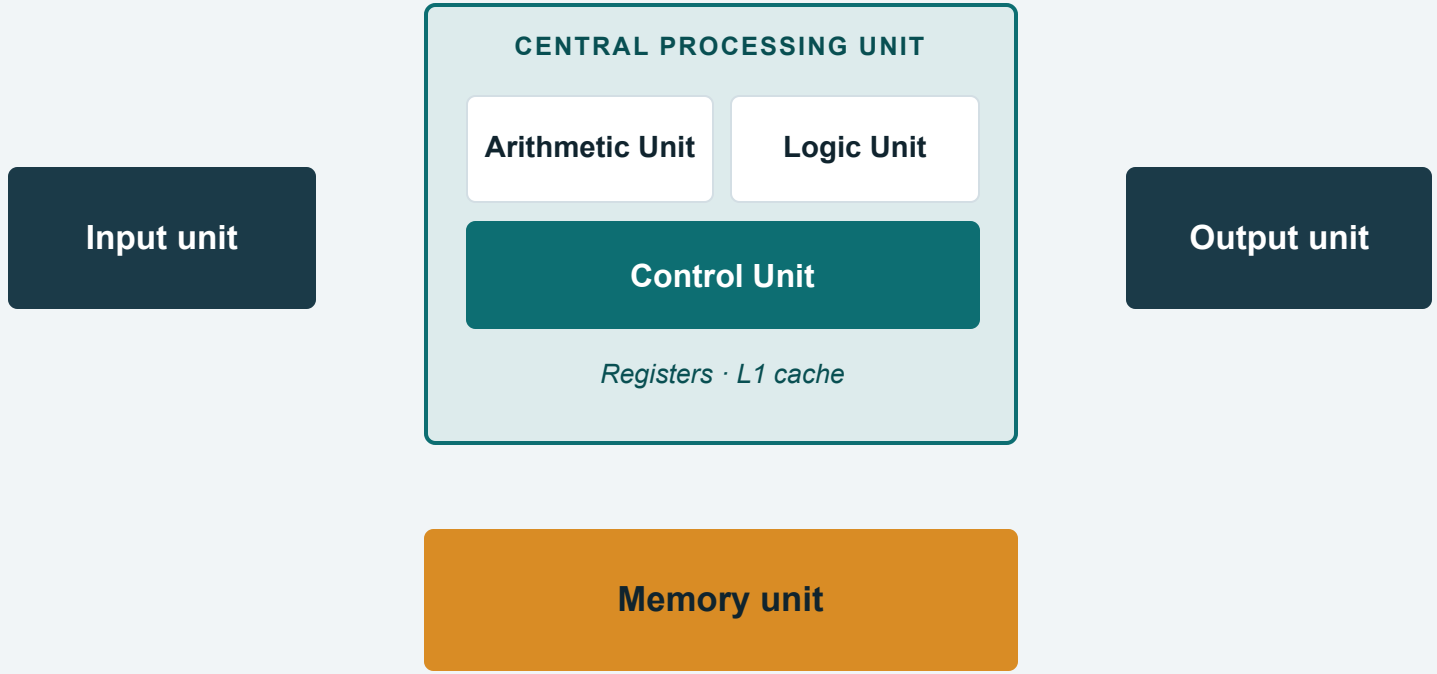
“The hardware units are arranged to work in tandem, in an orderly manner.”

Statement 4

Answers: 1 — architecture (the instruction set is one of its attributes). 2 — organisation (cost, physical size and technology decide the model). 3 — architecture. 4 — organisation.

FIG. 2.1

The block diagram of a computer system



Data flows in, is processed by the CPU, and flows out. Memory serves the CPU throughout.

The CPU is the central component the whole system revolves around.

It processes the data
The CPU is responsible for processing the data inside the computer system.

It controls everything else
It is also responsible for controlling all the other components of the system.

Three units do the work: Arithmetic Unit · Logic Unit · Control Unit.
Three memory subsystems support them: main memory · cache memory · registers.

FIG. 2.2

The CPU cycle — four operations, over and over

1 Fetch

Fetch the instruction from the memory.

2 Decode

Decode the instruction to decide what operations are to be performed.

3 Execute

Execute the instruction.

4 Store

Store the result back in the memory.

This four-phase process is known as the CPU cycle. Later in the lesson the chapter describes the machine cycle, which has these same four phases, and we break each one into more detail.

The CPU consists of three subsystems

Arithmetic Unit (AU) **Logic Unit (LU)** **Control Unit (CU)**

…and uses three memory subsystems: main memory unit · cache memory · registers.

Arithmetic Unit — the part that calculates

The Arithmetic Unit performs arithmetic operations on the data: addition, subtraction, multiplication and division.

Multiplication and division

Usually implemented as a repetitive process of addition and subtraction respectively.

Separate units

Some CPUs contain separate AUs for integer or fixed-point operations and for real or floating-point operations.

Where the result goes

The output is stored in a storage register by the AU. A register is a small storage area inside the CPU from where data is retrieved faster than from any other storage area.

The AU takes its input as an instruction made of three parts

Opcode

Specifies the operation to be performed

Operands

Specify the data on which the operation is to be performed

Format code

Suggests the format of the operands — fixed-point or floating-point

Logic Unit and Control Unit

Logic Unit (LU)

Performs logical operations on the data — 16 different types of logical operation in all.

greater than >	**less than <**
equal to =	**not equal to ≠**
shift left	**shift right**

To do this, the LU makes use of logic gates such as AND, OR and NOR.

Control Unit (CU)

Controls the flow of data and information, and maintains the sequence of operations being performed by the CPU.

1. Fetches an instruction from the storage area, decodes it and transmits the signals to the AU or LU and the storage registers
2. Guides the AU and LU about the operations to be performed
3. Suggests the I/O devices to which the data is to be communicated
4. Uses a program counter register to retrieve the next instruction, and a status register for conditions such as overflow of data

CHECK FOR UNDERSTANDING

Which unit? · call it out

Which part of the CPU would do each of these?

1

Work out 47 × 3.

Job 1

2

Decide whether one value is greater than another.

Job 2

3

Fetch the next instruction and tell the other units what to do.

Job 3

4

Hold the result that has just been calculated.

Job 4

Answers: 1 — the Arithmetic Unit. 2 — the Logic Unit. 3 — the Control Unit. 4 — a register (the AU stores its output in a storage register). Follow-up: how would the AU actually carry out job 1?

02

The Memory the CPU Uses

Main memory · cache memory · registers — three subsystems, each faster and smaller than the last

Main memory (RAM)

Cache memory

L1 and L2

Registers

Main memory — fast, limited and temporary

Also called: internal memory · primary memory · Random Access Memory (RAM)

1

Temporary

A temporary storage medium that holds data only for a short period of time. Once the computer is switched off, the data stored in RAM gets erased.

2

Limited

The memory space of RAM is limited, so not all files and instructions can be stored in it.

3

Swapping

Files and instructions normally live in secondary storage and are copied from there into RAM before execution. This technique is called swapping.

4

It affects speed

More memory space means more instructions can be copied and executed at the same time, so the system does not have to read from secondary storage again and again.

Main memory is also responsible for holding intermediate data transferred between the CPU and the I/O devices.

Cache memory — small, fast and expensive

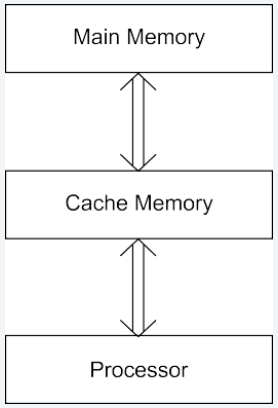


Fig. 2.3 The cache memory sits between the CPU and main memory

The transfer of data between the processor and the cache memory is bidirectional.

A small, fast and expensive memory that stores copies of the data that needs to be accessed frequently from the main memory.

Before reading or writing

The processor checks the cache for the same data before going to the main memory.

If the data is there

It reads from or writes to the cache itself, because the cache's access time is much faster than the main memory's.

Cache hit

The availability of data in the cache is known as a cache hit. The capability of a cache memory is measured on the basis of cache hit.

Two levels of cache

Primary cache

LEVEL 1 (L1) CACHE · INTERNAL CACHE

Where	Located inside the CPU
Size	Smaller
Speed	The fastest type of cache
Purpose	Gives quick access to the data most frequently used by the microprocessor

Secondary cache

LEVEL 2 (L2) CACHE · EXTERNAL CACHE

Where	Located outside the CPU, normally on the motherboard
Size	Larger
Speed	Slower than the primary cache
Also	Larger than the primary cache, so it holds more of the frequently used data

Remember the trade-off: L1 is smaller but faster; L2 is larger but slower.

Registers — six you must know by name

A few special purpose, temporary storage units inside the CPU. They are high-speed memory locations that hold instructions, data and intermediate results currently being processed.

PC — **Program Counter**

Keeps track of the next instruction to be executed.

IR — **Instruction Register**

Holds instructions to be decoded by the control unit.

MAR — **Memory Address Register**

Holds the address of the next location in memory to be accessed.

MBR — **Memory Buffer Register**

Stores data received from or sent to the CPU.

MDR — **Memory Data Register**

Stores operands and data.

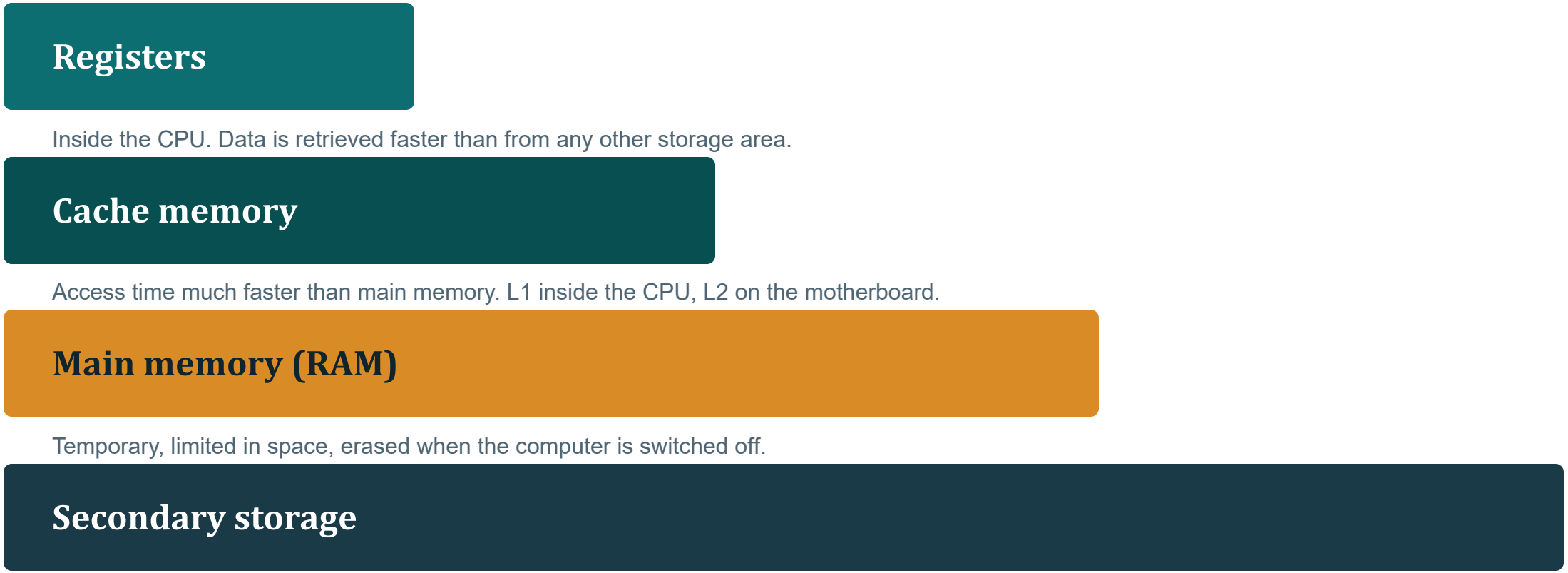
ACC — **Accumulator**

Stores the results produced by the arithmetic and logic units.

Many computers employ additional registers. The number and sizes of registers vary from processor to processor, and an effective implementation of registers can considerably increase the speed of the processor.

Why a computer needs several kinds of memory

Faster and smaller at the top; larger and slower at the bottom. The bar widths show relative capacity, not measured figures.



CHECK FOR UNDERSTANDING

Name the register · write it down

Which register or memory is being described?

1

It keeps track of the next instruction to be executed.

Clue 1

2

It holds the address of the next location in memory to be accessed.

Clue 2

3

It stores the results produced by the arithmetic and logic units.

Clue 3

4

It is small, fast and expensive, and the processor checks it first.

Clue 4

Answers: 1 — the Program Counter (PC). 2 — the Memory Address Register (MAR). 3 — the Accumulator. 4 — cache memory.

03

Internal Communications

How the processor talks to memory, and how it talks to input and output devices

- Two categories
- Memory read & write
- The interface unit
- I/O read & write

Two ways the processor communicates

The CPU communicates with memory and with the I/O devices in order to transfer data between them — but the method is different for each.

Processor to memory

The CPU may communicate with the memory either directly or through the cache memory.

Direct communication is implemented with the help of two registers: the Memory Address Register (MAR) and the Memory Buffer Register (MBR).

- **Memory read**
- **Memory write**

Processor to I/O devices

Communication with I/O devices is usually implemented with the help of interfaces.

Each input and output device is provided with a device controller. The processor communicates with those controllers through an interface unit.

- **I/O read**
- **I/O write**

FIG. 2.4

Processor to memory — two registers do the work

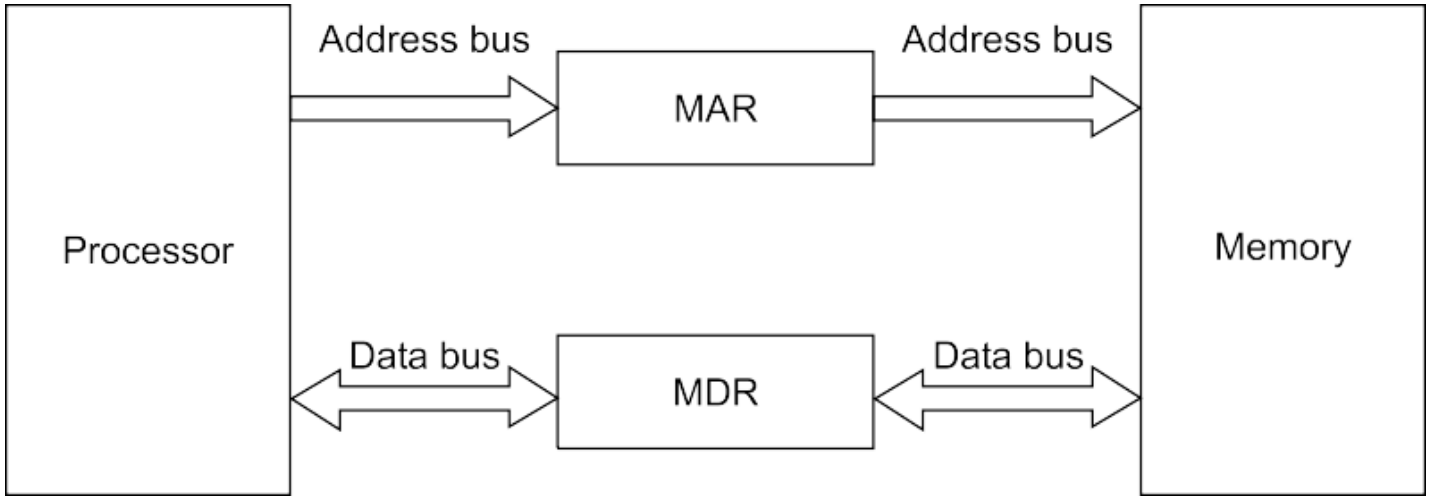


Fig. 2.4 Communication between the processor and the memory

Address bus Carries the address out from the processor, through MAR, to the memory.

Data bus Carries the data between MDR and both sides — in either direction.

MAR **Memory Address Register**

Used by the processor to keep track of the memory location where it needs to read or write. It holds the address of the memory location.

MDR **Memory Data Register**

Used by the processor to store the data that needs to be transferred to or from the memory.

The two operations are called the memory read and the memory write.

FIG. 2.5

Memory read — four steps

The processor performs these steps to read the data from the desired memory location.

1. The processor loads the address of the memory location from where data is to be read into the MAR register, using the address bus.
2. The processor issues the READ control signal through the control bus.
3. After receiving the READ signal, the memory loads the data into the MDR register from the location specified in MAR, using the data bus.
4. Finally, the data is transferred to the processor.

The control bus carries the commands issued by the processor, and the status signals generated by the various devices in response to those commands.

FIG. 2.6

Memory write — four steps

The processor performs these steps to write the data at the desired memory location.

1. The processor loads the address of the memory location where data is to be written in the MAR register, using the address bus.
2. The processor loads the desired data in the MDR register, using the data bus.
3. The processor issues the WRITE control signal to the memory, using the control bus.
4. Finally, the memory stores the data loaded in the MDR register at the desired memory location.

Spot the difference: in a read, the control signal comes second and the data arrives last. In a write, the data is loaded second and the control signal comes third.

CHECK FOR UNDERSTANDING

Put it in order · work in pairs

These four steps of a memory read are jumbled. What is the correct order?

1

The memory loads the data into MDR from the location specified in MAR.

Step A

2

The data is transferred to the processor.

Step B

3

The processor loads the address into MAR, using the address bus.

Step C

4

The processor issues the READ control signal through the control bus.

Step D

Answer: C → D → A → B. Follow-up: change one step to turn this into a memory write. (Step D becomes the WRITE signal — and it moves to third place, after the data is loaded into MDR.)

FIG. 2.7

Processor to I/O devices — through an interface unit

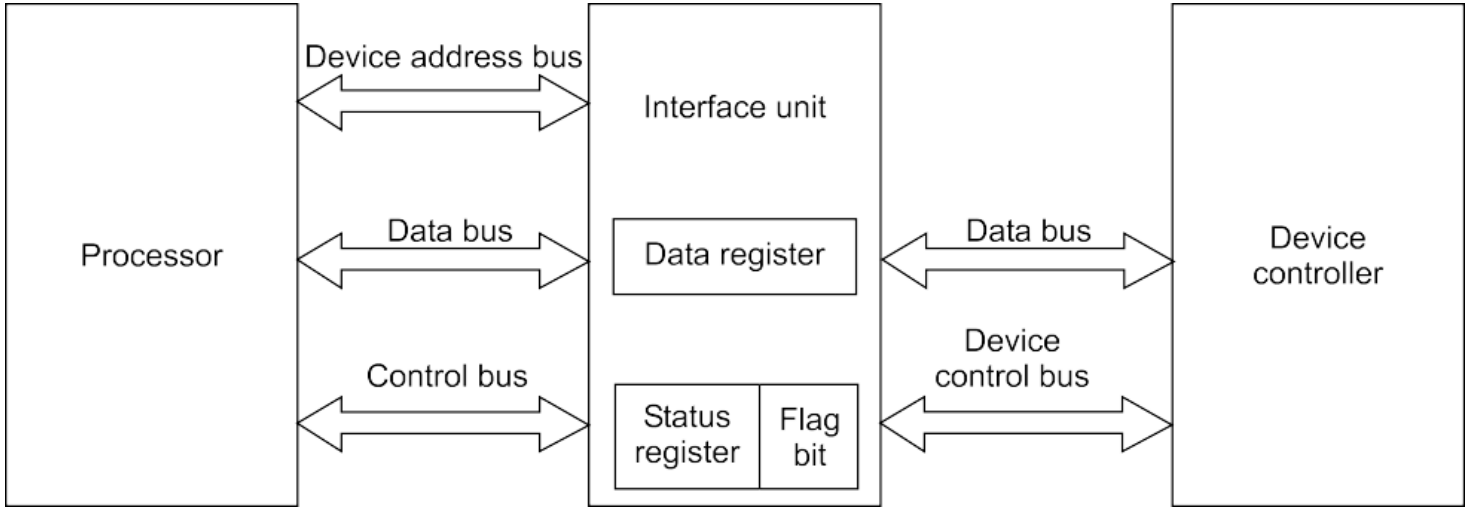


Fig. 2.7 The processor, the interface unit and the device controller

I/O read The processor reads the data from an input device.

I/O write The processor writes the data to an output device.

The interface unit is responsible for controlling the input and output operations between the processor and the I/O devices.

Device controller
Every input and output device has one. It manages that device's working.

Interface unit
The intermediary. It interprets the processor's control commands so the device controllers can act on them.

Data register
Stores the data to be transferred — to the processor, or to an output device.

Status register
Shows whether the data register is holding data. If it is, the flag bit is set to one.

FIG. 2.8

I/O read — data from an input device to the processor

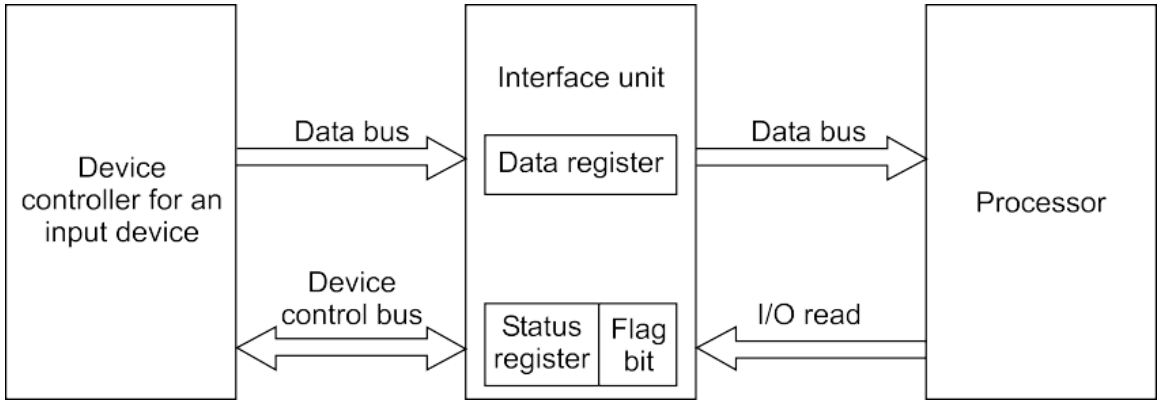


Fig. 2.8 The I/O read operation

Notice the handshake.
Every transfer is confirmed: data valid → data accepted → acknowledgement. Neither side assumes the other is ready.

1. The input device places the data on the data bus — a single byte at a time.
2. The input device issues the data valid signal through the device control bus to the data register.
3. When the data register accepts the data it issues a data accepted signal back, and the input device then disables the data valid signal.
4. The flag bit F of the status register is set to 1, because the data register now holds the data.
5. The processor issues an I/O read signal to the data register in the interface unit.
6. The data register places the data on the data bus to the processor, which acknowledges that the data has been received.

FIG. 2.9

I/O write — data from the processor to an output device

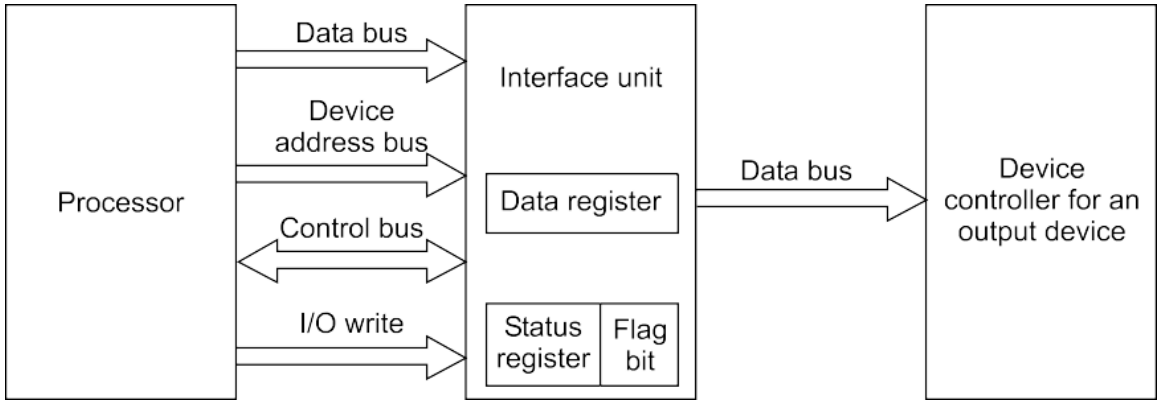


Fig. 2.9 The I/O write operation

Compare with the I/O read.
Here the processor starts the conversation and must also supply the device's address — an input device announced itself instead.

1. The processor places the data on the data bus connected to the data register of the interface unit.
2. The CPU places the address of the output device on the device address bus.
3. The CPU issues the I/O write signal, which writes the data on the data register; the flag bit is set to 1.
4. The data register issues a data accepted signal through the control bus to the processor.
5. The interface unit places the data from the data register on to the data bus connected to the device controller.
6. The output device receives the data and sends an acknowledgement back to the processor through the interface unit.

CHECK FOR UNDERSTANDING

True or false · hands up

True or false? Decide before I reveal.

1

The processor communicates with an I/O device directly, without any interface.

Statement 1

2

The flag bit of the status register is set to 1 when the data register holds the data.

Statement 2

3

An input device transfers a single byte of data at a time.

Statement 3

4

On an I/O write, the CPU places the address of the output device on the device address bus.

Statement 4

Answers: 1 — FALSE, communication with I/O devices is implemented with the help of interfaces. 2 — TRUE. 3 — TRUE. 4 — TRUE.

REVIEW

Eight questions before we finish

1. What is the difference between computer architecture and organisation?
2. Which unit of the CPU performs all the arithmetic operations?
3. Which register keeps track of the next instruction to be executed?
4. Which memory does the CPU check first when searching for data?
5. Which cache is also known as the internal cache, and where is it located?
6. Which two registers implement direct processor-to-memory communication?
7. Name the four steps of a memory write, in order.
8. Which unit is the intermediary between the processor and a device controller?

REVIEW

Answers

1 **What it is vs how it is built**

Architecture defines the attributes and logical structure; organisation is the physical arrangement of the units.

2 **The Arithmetic Unit**

Addition, subtraction, multiplication and division.

3 **The Program Counter (PC)**

The Control Unit uses it to retrieve the next instruction.

4 **Cache memory**

It is checked before reading from or writing to the main memory.

5 **Primary cache — L1**

Located inside the CPU. Smaller but the fastest type of cache.

6 **MAR and MBR**

MAR holds the address; the data register — MBR, shown as MDR in the figures — holds the data.

7 **MAR → MDR → WRITE → store**

Address into MAR, data into MDR, the WRITE signal on the control bus, then memory stores the data.

8 **The interface unit**

It interprets the processor's commands so that device controllers can act on them.

EXIT TICKET

Answer these three before you leave

Write your answers on a slip of paper with your name and hand it in at the door.

1

In one sentence each, say what computer architecture is and what computer organisation is.

Tests objective 1

2

List the four steps of a memory read, in order.

Tests objective 4

3

Which register holds a result, and which holds the next memory address?

Tests objective 3

Next: five interactive activities — CPU components, the memory and I/O sequencer, CPU registers, identify the component, and the knowledge challenge.